Notice of Allowability	Application No.	Applicant(s)	
	10/765,488	BHAKTA ET AL.	
	Examiner	Art Unit	
	Ly D. Pham	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *01 November 2004 and 31 January 2005*.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☒ The drawings filed on *27 January 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 110104
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

DETAILED ACTION

1. Applicant's Request for Reconsideration filed November 01, 2004 has been entered.

2. Applicant's Information Disclosure Statement, IDS, filed November 01, 2004 has been considered by the examiner.

3. This application is in condition for allowance except the following formal matter.

EXAMINER'S AMENDMENT

4. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Bruce S. Itchkawitz (reg. no. 47, 677) on January 31, 2005.

The application has been amended as follows:

i. Replace claims 1, 8, 9, 11, 18, and 19 with the following amended version.

1. A memory module comprising:

a printed circuit board having a first lateral portion and a second lateral portion;

a plurality of identical integrated circuits mounted in a first row and a second row onto at least one surface of the printed circuit board;

a control logic bus connected to the plurality of identical integrated circuits, the control logic bus comprising a first set of address signal paths and a second set of address signal paths; and

a first register and a second register connected to the control logic bus, the first register accessing a first rang and a second range of data bits, the second register accessing the third range and a fourth range of data bits, the first range and the second range of data bits being first and second non-contiguous subsets of a data word, and the third range and the fourth range of data bits being third and fourth non-contiguous subsets of data word, wherein the first set of address signal paths connect the first register to the integrated circuits of the first row and the second row on the first lateral portion and the second set of address signal paths connect the second register to the integrated circuits of the first row and the second row on the second lateral portion.

8. The memory module of claim 3, wherein the first set of address signal paths connect the integrated circuits of the first row on the first lateral half to the first register and the second set of address signal paths connect the integrated circuits of the first row and the second row on the second lateral half to the second register, the first set of address signal paths and the second set of

address signal paths being bilaterally symmetric to one another across the line of bilateral symmetry.

9. The memory module of claim 1, wherein the first register address the identical integrated circuits located in the first row and in the second row on the first lateral portion of the printed circuit board, and the second register addresses the identical integrated circuits located in the first row and in the second row on the second lateral portion of the printed circuit board.

11. A method of accessing data bits of a data word, the method comprising:

providing a memory module comprising:

a printed circuit board having a first lateral portion and a second lateral portion;

a plurality of identical integrated circuits mounted in a first row and a second row onto at least one surface of the printed circuit board;

a control logic bus connected to the plurality of identical integrated circuits, the control logic bus comprising a first set of address signal paths connected to the integrated circuits of the first row and the second row on the first lateral portion and a second set of address signal paths connected to the integrated circuits of the first row and the second row on the second lateral portion; and

a first register and a second register connected to the control logic bus, wherein the first register is connected to the integrated circuits of the first row and the second row on the first lateral portion by the first set of address signal paths and the second register is connected to the integrated circuit of the first row and the second row on the second lateral portion by the second set of address signal paths;

accessing a first range of data bits and a second range of data bits using the first register, the first range and the second range of data bits being first and second non-contiguous subsets of the data word; and

accessing a third range of data bits and a fourth range of data bits using the second register, the third range and the fourth range of data bits being third and fourth non-contiguous subsets of the data word.

18. The method of claim 13, wherein the first set of address signal paths connect the integrated circuits of the first row and the second row on the first lateral half to the first register and the second set of address signal paths connect the integrated circuits of the first row and the second row on the second lateral half to the second register, the first set of address signal paths and the second set of address signal paths being bilaterally symmetric to one another across the line of bilateral symmetry.

19. The method of claim 11, wherein the first register addresses the identical integrated circuits located in the first row and in the second row on the first lateral portion of the printed circuit board, and the second register addresses the identical integrated circuits located in the first row and in the second row on the second lateral portion of the printed circuit board.

ii. Cancel claim 21.

Conclusion

5. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ly D. Pham whose telephone number is 571-272-1793. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ly Pham
February 1, 2005

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Technology Center 2800